REMARKS

Claims 1-20, 27-37, 41-43, 45, 46, 48-53, and 57-60 are in the current application.

Claims 21-26, 38-40, 44, 47, and 54-56 are cancelled without prejudice by this amendment.

New claims 57-60 are added by this amendment to more particularly point out other equivalents.

First 35 USC 102 Rejection:

Claims 21-27 and 32 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. patent no. 6,094,039 issued to Farrenkopf. This rejection is respectfully traversed. As allowed under 35 USC 251 and 252, claims 21-56 were submitted to correct a defect in Applicants' originally issued patent. Thus, claims 21-56 and 32 are supported by the specification of the originally filed application and are a part of the originally filed application. Thus, claims 21-56 and 32 are entitled to at least Applicants' original filing date of June 4, 1997. The Farrenkopf patent has a filing date of October 15, 1999. Applicants' June 4, 1997 filing date pre-dates that of the Farrenkopf reference, thus, the Farrenkopf patent should be removed as a reference.

Additionally, claims 21-26 are cancelled by this amendment, thus, the rejection thereof is now moot. Since Farrenkopf is removed as a reference, the cancellation of claims 21-26 is not related to the statutory requirements of patentability and is not made to distinguish over a particular reference or combination of references.

Accordingly, it is respectfully submitted that the rejection of claims 21-27 and 32 over Farrenkopf should be withdrawn.

Second 35 USC 102 Rejection:

Claims 27-30 and 32 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent no. 5,313,381 issued to Balakrishnan, or 4,146,832 issued to McConnell. This rejection is respectfully traversed.

Referring to the Balakrishnan reference (the '381 patent), applicants' amended claim 27 calls for, among other things, providing a control signal to the integrated regulator circuit which alters the switching signal of the integrated regulator circuit over multiple cycles of the switching signal wherein the control signal is received externally to the integrated regulator circuit. The '381 patent discloses using only three terminals; a feedback, a ground, and a switching signal output. Since claim 27 calls for both a feedback and a control signal received externally to the integrated regulator circuit, the '381 patent can not disclose at least this element of claim 27. Accordingly, it is respectfully submitted that the '381 patent is deficient in anticipating claim 27.

Claims 28-30 depend from claim 27 and are believed to be allowable for at least the same reasons as claim 27.

Still referring to the Balakrishnan reference, applicants amended claim 32 calls for at least, a state circuit having an input coupled for receiving a control signal from external to the regulator circuit, and

a memory circuit coupled to receive a state of the control signal and responsively store a mode of operation of the regulator circuit. As indicated in the discussion of the claim 27 rejection, the '381 patent is silent on receiving a control signal externally to the regulator circuit and storing a mode of operation of the regulator circuit responsively to a state of the externally received

control signal. Accordingly, it is respectfully submitted that the '381 patent can not anticipate amended claim 32.

Referring to the McConnell reference, applicants' amended claim 27 calls for, among other things, storing a mode of operation of the integrated regulator circuit in a memory circuit. The McConnell reference is silent on a memory circuit of any kind, much less, storing a mode of operation in the memory circuit. Accordingly, it is respectfully submitted that the McConnell reference can not anticipate amended claim 27.

Claims 28-30 depend from claim 27 and are believed to be allowable for at least the same reasons as claim 27.

Still referring to the McConnell reference, applicants' amended claim 32 calls for at least, a memory circuit coupled to receive a state of the control signal and responsively store a mode of operation of the regulator circuit. The McConnell reference is silent on a memory circuit of any type much less one that is coupled to receive a state of the control signal and responsively store a mode of operation of the regulator circuit. Accordingly, it is respectfully submitted that the '832 patent can not anticipate amended claim 32.

Third 35 USC 102 Rejection:

Claims 32-37 and 45 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent no. 4,425,612 issued to Bahler et al, or 4,301,497 issued to Johari. This rejection is respectfully traversed. A

Referring to the Bahler et al reference, applicants' amended claim 32 calls for, among other features, an integrated circuit containing a regulator circuit, the

regulator circuit comprising a state circuit having an input coupled for receiving a control signal from external to the regulator circuit and an output for providing a mode signal in response to the control signal; a switching regulator circuit and a memory circuit. Bahler et al do not disclose an integrated circuit that has all three elements: a control circuit, a switching regulator, and a memory circuit on the integrated circuit. Accordingly, it is respectfully submitted that claim 32 can not be anticipated by the Bahler et al reference.

Claims 33-37 depend from claim 32 and are believed allowable for at least the same reasons as claim 32.

Referring still to the Bahler et al reference, applicants' amended claim 45 includes a semiconductor chip having a regulator circuit formed to provide a drive signal used to regulate power transfer of a power supply in response to a feedback signal and formed to receive an external control signal used to suspend power transfer of the power supply, a memory circuit having a first input coupled to an output of a comparator for setting an output state of the memory circuit as the mode signal according to a value of the external control signal, and a switching regulator circuit. Bahler et al are silent on a semiconductor chip that has a regulator circuit and a memory circuit on the semiconductor chip to regulate the power transfer. Additionally, Bahler et al are also silent on receiving the external control signal to suspend power transfer. Bahler et al disclose modifying the on-time and off-time to increase or decrease the amount of power in anticipation of an expected power load (see column 4, lines 16-19), however, Bahler et al are silent on suspending power transfer as called for in claim 45. Accordingly, it is

respectfully submitted that the Bahler et al reference is deficient in anticipating claim 45.

Referring to the Johari reference, applicants' amended claim 32 calls for, among other features, an integrated circuit containing a state circuit, a switching regulator circuit, and a memory circuit. Johari is silent on a memory circuit. Additionally, Johari does not disclose an integrated circuit that has a control circuit, a switching regulator, and a memory circuit on the integrated circuit. At least these element of claim 32 are not disclosed by Johari. Accordingly, it is respectfully submitted that the Johari reference can not anticipate claim 32.

Claims 33-37 depend from claim 32 and are believed allowable for at least the same reasons as clam 32.

Still referring to the Johari reference, applicants amended claim 45 calls for at least a semiconductor chip having a regulator circuit formed to provide a drive signal used to regulate power transfer of a power supply in response to a feedback signal and formed to receive an external control signal used to suspend power transfer of the power supply, a memory circuit having a first input coupled to an output of a comparator for setting an output state of the memory circuit as the mode signal according to a value of the external control signal, and a switching regulator circuit. Johari is silent on a memory circuit. Johari is also silent on a semiconductor chip that has a regulator circuit, a control circuit, and a memory circuit on the semiconductor chip to regulate the power transfer. Additionally, Johari is also silent on setting an output state of the memory circuit according to a value of the control signal. At least these elements of claim 45 are not disclosed by the Johari reference. Accordingly, it is

respectfully submitted that amended claim 45 can not be anticipated by the Johari reference.

Fourth 35 USC 102 Rejection:

Claims 38-50 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent no. 5,610,503 issued to Fogg et al. This rejection is respectfully traversed.

Claims 38-40 are cancelled by this amendment, thus, the rejection thereof is now moot.

Applicants' amended claim 41 calls for, among other features, a memory circuit having a first input coupled to receive a state of the operating mode control signal from an output of a comparator and responsively set an output state of the memory circuit to set the mode of operation. Fogg et al are silent on having an input of a memory circuit coupled to an output of a comparator, much less having the memory input coupled to the comparator output to receive an operating state of the operating mode control signal. Thus the couplings called for by at least this element of claim 41 are not disclosed by Fogg et al. Accordingly, it is respectfully submitted that amended claim 41 is not anticipated by Fogg et al.

Claims 42-43 depend from claim 41 and are believed to be allowable for at least the same reasons as claim 41. Additionally, Fogg is silent on the couplings required by claim 43. Accordingly, it is respectfully submitted that claims 42-43 can not be anticipated by the Fogg et al reference.

Claim 44 is cancelled by this amendment.

Amended claim 45 calls for, among other features, a memory circuit having a first input coupled to an output of a comparator for setting an output state of the memory circuit. At least this element of claim 45 is not disclosed

by Fogg et al. Accordingly, it is respectfully submitted that Fogg et al can not anticipate amended claim 45.

Claims 46 and 48-50 depend from claim 45 and are believed to be allowable for at least the same reasons as claim 45.

Claim 47 is cancelled by this amendment.

Additionally, amended claim 46 calls for the comparator having a first input coupled for receiving the external control signal, a second input coupled for receiving a first reference signal, and the output coupled to the first input of the memory circuit. These comparator couplings are not disclosed by Fogg et al.

Further, amended claim 50 includes a first and a second comparator coupled to first and second inputs of the memory circuit. Fogg et al are silent on a first and a second comparator coupled to first and second memory inputs.

Accordingly, it is respectfully submitted that amended claims 46 and 48-50 are not anticipated by Fogg et al.

Fifth 35 USC 102 Rejection:

Claims 38 and 45-56 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent no. 4,823,070 issued to Nelson. This rejection is respectfully traversed.

Claim 38 is cancelled by this amendment, thus, the rejection thereof is now moot.

Amended claim 45 includes, among other things, wherein the state circuit includes a memory circuit having a first input coupled to an output of a comparator for setting an output state of the memory circuit as the mode signal according to a value of the external control signal; and a switching regulator circuit. Nelson discloses a switching regulator circuit 100 (column 4, lines 59-60) that has a flip-flop 106 that is used a part of the switching portion of regulator 100. Flip-flop 106 is a well-know element of a

switching regulator circuit. However, Applicants' amended claim 45 calls for a switching regulator circuit in addition to a state circuit that has a memory circuit having a first input coupled to an output of the comparator for setting an output state of the memory circuit. Consequently flip-flop 106 disclosed by Nelson can not be the memory circuit called for by amended claim 45. Accordingly, it is respectfully submitted that claim 45 can not be anticipated by the Nelson reference.

Claims 46, and 48-50 depend from claim 45 and are believed to be allowable for at least the same reasons as claim 45.

Claim 47 is cancelled by this amendment.

Additionally, amended claim 50 calls for a first and a second comparator coupled to a respective first and second inputs of the memory circuit. Nelson is silent on such a coupling to the memory circuit.

Applicants' amended claim 51 calls for, among other things, a state circuit external to the switching regulator, the state circuit having a memory circuit coupled to set an output state of the memory circuit responsively to a state of the mode control signal. Nelson discloses a switching regulator circuit 100 (column 4, lines 59-60) that has a flip-flop 106 that is used a part of the switching portion of regulator 100. Flip-flop 106 is a well-know element of a switching regulator circuit. However, Applicants' amended claim 51 calls for a state circuit external to the switching regulator, the state circuit having a memory circuit. Consequently flip-flop 106 disclosed by Nelson can not be the memory circuit called for by amended claim 51. Accordingly, it is respectfully submitted that the Nelson reference can not anticipate claim 51.

Claims 52 and 53 depend from claim 51 and are believed to be allowable for at least the same reasons as claim 51.

Claims 54-56 are cancelled by this amendment.

Sixth 35 USC 102 Rejection:

Claims 45-56 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent no. 5,490,055 issued to Boylan et al. This rejection is respectfully traversed.

Amended claim 45 calls for, among other things, wherein the state circuit includes a memory circuit having a first input coupled to an output of a comparator for setting an output state of the memory circuit as the mode signal according to a value of the external control signal. Boylan et al are silent on a memory circuit of any type. It should be noted that the Boylan et al capacitors 132 and 131 are connected to resistors as part of an analog integrator. The resistors will discharge any energy stored on the capacitors, thus, capacitors 131 and 132 can not be a memory circuit as required by claim 45. Accordingly, it is respectfully submitted that claim 45 can not be anticipated by Boylan et al.

Claims 46, and 48-50 depend from claim 45 and are believed to be allowable for at least the same reasons as claim 45.

Claim 47 is cancelled by this amendment.

Additionally, amended claim 50 calls for a first and a second comparator coupled to a respective first and second inputs of the memory circuit. Boylan et al are silent on such a coupling to the memory circuit.

Applicants' amended claim 51 calls for, among other things, a state circuit external to the switching regulator, the state circuit having a memory circuit coupled to set an

output state of the memory circuit responsively to a state of the mode control signal. As stated in the comments regarding claim 45, capacitors 131 and 132 of Boylan et al can not be a memory circuit as required by claim 51. Accordingly, it is respectfully submitted that Boylan et al are deficient in anticipating claim 51.

Claims 52 and 53 depend from claim 51 and are believed to be allowable for at least the same reasons as clam 51.

Claims 54-56 are cancelled by this amendment.

New claims 57-60;

New claims 57-60 depend from issued claim 8 and are believed to be allowable for at least the same reasons as issued claim 8. New claims 57-60 are supported by the specification and at least by FIG. 1 and FIG. 2. of the issued patent. Claims 57-60 contain no new matter.

Although it is believed that no fees are due for this amendment, the commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to deposit account no. 50-1086.

In view of all of the above, it is believed that applicants' claims are allowable, and that the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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Date: Dec. 11, 2003